IN THE CLAIMS

1-3. (Canceled).

4. (Currently Amended) The semiconductor device of ~~claims 2, 3 or~~ claim 8, wherein said p-type layers and said n-type layers are made of at least one selected from polysilicon, amorphous silicon, single-crystal silicon on a insulating layer, SiC and SiGe.

5. (Previously Presented) The semiconductor device of claim 8, wherein said p-type layers and said n-type layers are formed so as to have the same width and the same concentration of impurities, in the same conductivity type, respectively.

6. (Previously Presented) The semiconductor device of claim 8, wherein a diffusion region having a different conductivity type from that of said semiconductor layer is formed on the closest side to said protective diode of said transistor cells arranged, said diffusion region having no other diffusion region therein, and said source wiring contacted to the most inner layer of said protective diode is contacted to said diffusion region.

7. (Canceled).

8. (Currently Amended) A semiconductor device comprising:

an insulating gate field effect transistor comprising a plurality of transistor cells which are arranged in a semiconductor layer and connected in parallel; and

a protective diode connected between a gate and a source of said insulating gate field effect transistor to prevent breakdown due to a voltage greater than or equal to a particular value,

wherein said protective diode is formed as a bidirectional diode in which one or more closed ring-shaped p-type layers and one or more closed ring-shaped n-type layers are flatly and alternately provided on an insulating layer at a peripheral portion of a region of said transistor cells, a source wiring contacts with the most inner layer of said protective diode, and a closed ring-shaped metal film contacts with the most outer layer of said protective diode, said closed ring-shaped metal film being successively formed with a gate electrode pad comprising a metal film; [[and]]

wherein said ring-shaped metal film substantially contacts the full circumferential length of the most outer layer; and

wherein said ring-shaped metal film is a gate wiring which has gate connecting portions so as to connect to gate electrodes of said transistor cells with partial striding over said protective diode, and said gate connecting portions and source connecting portions of said source wiring which are contacted with said most inner layer are alternately formed in plan view.

9. (Canceled).